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Claims

[c1] A bipolar transistor, comprising:
a collector region;
an intrinsic base layer overlying said collector region;
an emitter overlying said intrinsic base layer;
an opened etch stop layer including a layer of dielectric material overlying said intrinsic base layer, said opened etch stop layer self-aligned to said emitter; and
a raised extrinsic base overlying said intrinsic base layer, said raised extrinsic base self-aligned to said emitter.

[c2] A bipolar transistor according to claim 1 wherein said emitter is disposed in an opening having a sublithographic dimension.

[c3] A bipolar transistor according to claim 1 wherein said emitter is disposed in contact with said intrinsic base layer, and said raised extrinsic base is spaced from said emitter by said opened etch stop layer where said emitter contacts said intrinsic base layer.

[c4] A bipolar transistor according to claim 3 wherein said opened etch stop layer consists essentially of at least one of an oxide and a nitride.

[c5] A bipolar transistor according to claim 4 further comprising a dielectric spacer overlying said opened etch stop layer, said dielectric spacer disposed between said raised extrinsic base and said emitter.

[c6] A bipolar transistor according to claim 5 wherein said opened etch stop layer consists essentially of an oxide and said dielectric spacer consists essentially of a nitride.

[c7] A heterojunction bipolar transistor (HBT) according to claim 1 wherein said intrinsic base layer includes a layer consisting essentially of a semiconductor alloy, such that said intrinsic base layer forms a heterojunction with at least said collector region.

[c8] An HBT according to claim 7 wherein said semiconductor alloy includes silicon germanium.

[c9] A bipolar transistor according to claim 1 wherein said raised extrinsic base includes a layer of semiconductor material and a low resistance layer disposed above said semiconductive layer, said low resistance layer including at least one material selected from metals and metal silicides.

[c10] A bipolar transistor according to claim 9 wherein said

low resistance layer includes said metal silicide.

[c11] A bipolar transistor according to claim 1, wherein said raised extrinsic base is disposed in conductive contact with said intrinsic base layer from within an opening in a dielectric layer.

[c12] A bipolar transistor according to claim 1, wherein a dimension of said opening is defined by photolithography.

[c13] A bipolar transistor according to claim 1 wherein a portion of said raised extrinsic base contacting said intrinsic base layer is disposed within an opening defined by photolithography within a layer consisting essentially of one or more materials selected from conductors and semiconductors.

[c14] A method of making a bipolar transistor (HBT), comprising:
forming a collector region;
forming an intrinsic base layer overlying said collector region;
forming a first layer of material overlying said intrinsic base layer;
defining a first opening in said first layer;
forming an etch stop layer overlying said intrinsic base layer within said first opening, said etch stop layer hav-

ing edges self-aligned to said first opening;
conformally depositing a raised extrinsic base material over said first material and inside said first opening to define a second opening wholly overlying said etch stop layer;
downwardly extending said second opening to said etch stop layer;
opening said etch stop layer;
forming an emitter within said second opening; and
forming a raised extrinsic base from said deposited raised extrinsic base material, said raised extrinsic base self-aligned to said emitter.

[c15] A method of making a heterojunction bipolar transistor (HBT) according to claim 14 wherein said intrinsic base layer is formed by a step including epitaxially growing a layer consisting essentially of a semiconductor alloy, such that said intrinsic base layer forms a heterojunction with at least said collector region.

[c16] A method as claimed in claim 14 wherein said second opening is extended downwardly by forming a dielectric spacer on a sidewall of said second opening and etching said etch stop layer from a bottom of said second opening.

[c17] A method as claimed in claim 14 wherein said step of

forming said raised extrinsic base includes forming a low resistance layer contacting said deposited raised extrinsic base material, said low resistance layer including at least one material selected from metals and metal silicides.

[c18] A method as claimed in claim 17 wherein said low resistance layer includes a metal silicide.

[c19] A method as claimed in claim 14, wherein said first layer of material consists essentially of a dielectric material.

[c20] A bipolar transistor according to claim 14 wherein said first opening is defined photolithographically, and said first layer consists essentially of one or more materials selected from conductors and semiconductors.